

Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan



FC8V22300L

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

- Source-source ON Resistance: $R_{ss(on)}$ typ. = 15 m Ω (VGS = 4.5 V)
- Built-in gate resistor
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: 4J

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

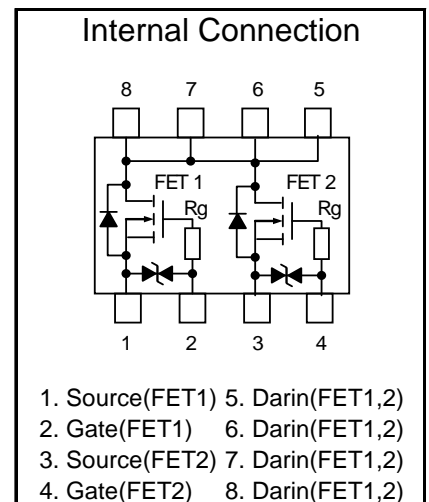
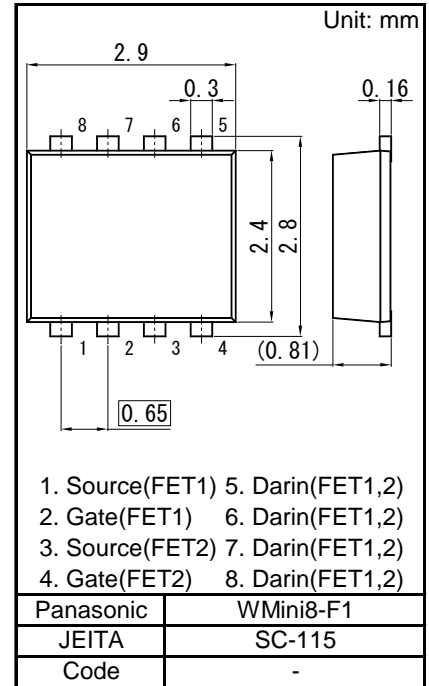
Parameter	Symbol	Rating	Unit	
Drain-source Voltage	VDS	20	V	
Gate-source Voltage	VGS	± 12	V	
Source Current	DC ^{*1}	IS1	6.5	A
	DC ^{*2}	IS2	9.5	A
	Pulse ^{*3}	ISp	65	A
Total Power Dissipation	$T_a = 25\text{ }^\circ\text{C}$, DC ^{*1}	PD1	1.0	W
	$T_a = 25\text{ }^\circ\text{C}$, DC ^{*2}	PD2	2.0	
	$T_a = 25\text{ }^\circ\text{C}$, $t = 10\text{ s}^{\text{*1}}$	PD3	1.2	
Channel Temperature	Tch	150	$^\circ\text{C}$	
Storage Temperature Range	Tstg	-55 to +150	$^\circ\text{C}$	
Thermal Resistance (ch-a)	Rth(ch-a)	125	$^\circ\text{C/W}$	

Note *1 Mounted on FR4 board (25.4 mm \times 25.4 mm \times t0.8 mm)

using the minimum recommended pad size (36 μm Copper).

*2 Mounted on Ceramic substrate (70 mm \times 70 mm \times t1.0 mm).

*3 $t = 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$



■ Electrical Characteristics Ta = 25 °C ± 3 °C

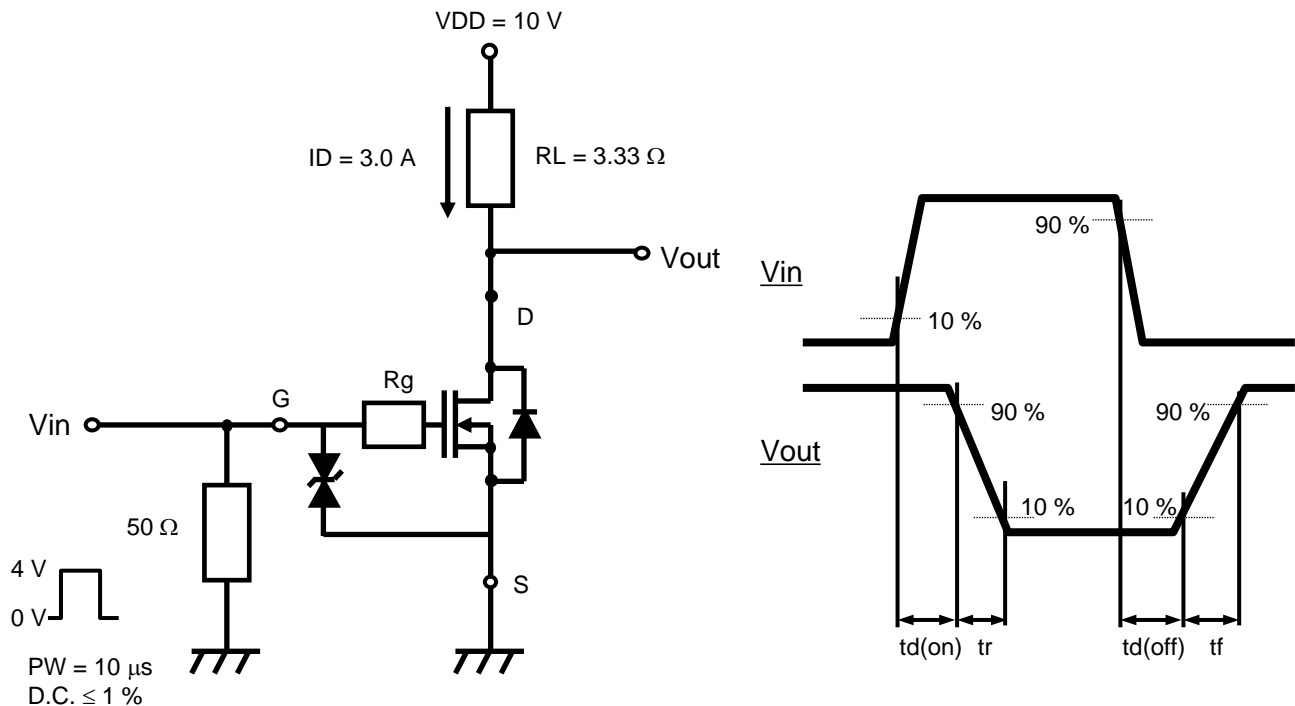
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Drain Current	IDSS	VDS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±1.0	μA
Gate-source Threshold Voltage	Vth	ID = 0.3 mA, VDS = 10 V	0.35	0.9	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 3.0 A, VGS = 4.5 V	10.5	15	20	mΩ
	RSS(on)2	IS = 3.0 A, VGS = 3.8 V	11	16	21.5	
	RSS(on)3	IS = 3.0 A, VGS = 3.1 V	11	17	28	
	RSS(on)4	IS = 3.0 A, VGS = 2.5 V	12	20	39	
Body Diode Forward Voltage	VSD	IF = 3.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance ^{*1}	Ciss	VDS = 10 V, VGS = 0 V, f = 1 KHz		830		pF
Output Capacitance ^{*1}	Coss			100		
Reverse Transfer Capacitance ^{*1}	Crss			80		
Turn-on delay Time ^{*1,*2}	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		0.2		μs
Rise Time ^{*1,*2}	tr	ID = 3.0 A		0.45		
Turn-off delay Time ^{*1,*2}	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		1.45		μs
Fall Time ^{*1,*2}	tf	ID = 3.0 A		0.95		
Total Gate Charge ^{*1}	Qg	VDD = 10 V		8		nC
Gate-source Charge ^{*1}	Qgs	VGS = 0 to 4.0 V,		3		
Gate-drain Charge ^{*1}	Qgd	ID = 3.0 A		2.5		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

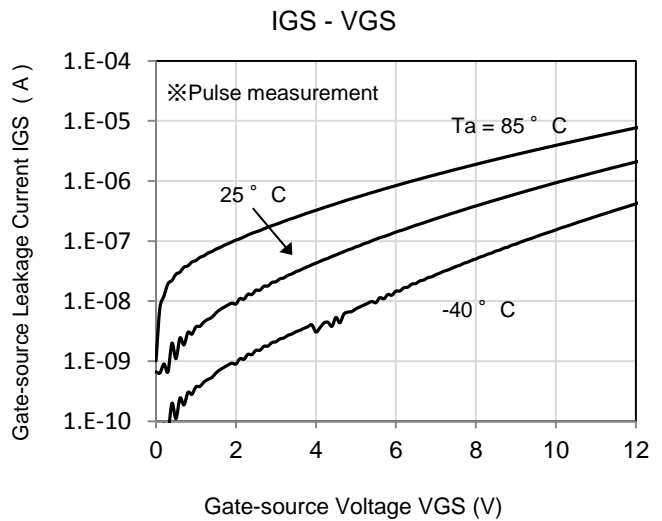
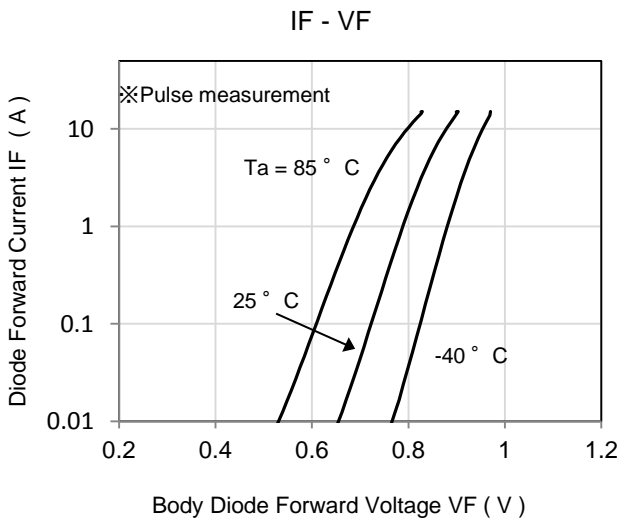
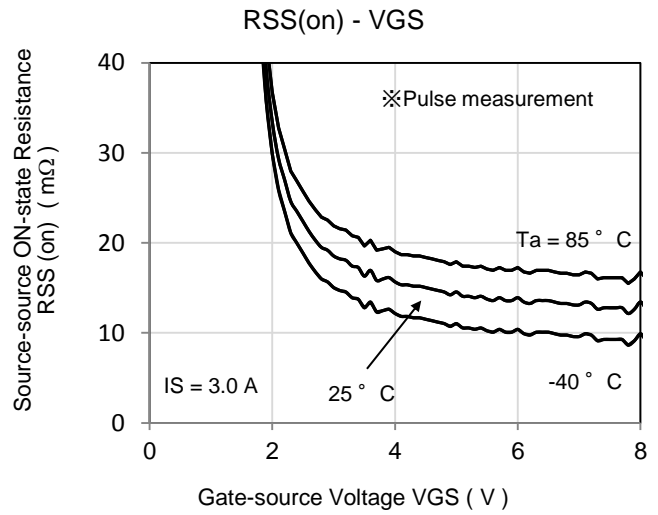
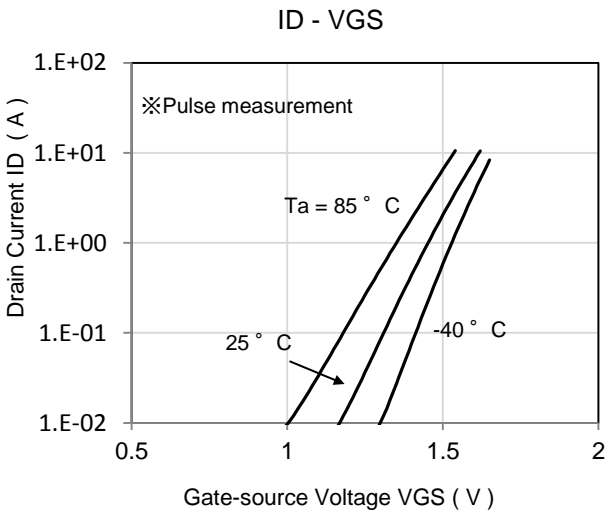
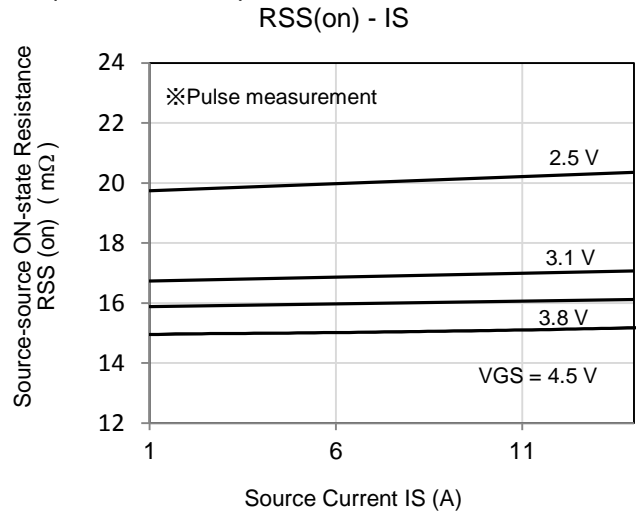
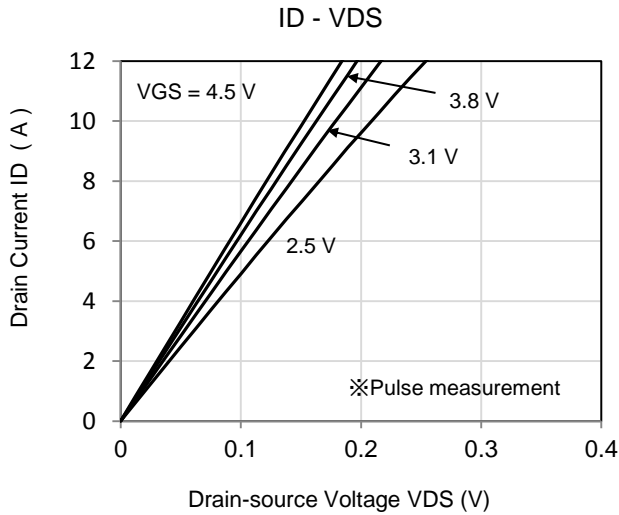
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2: Measurement circuit

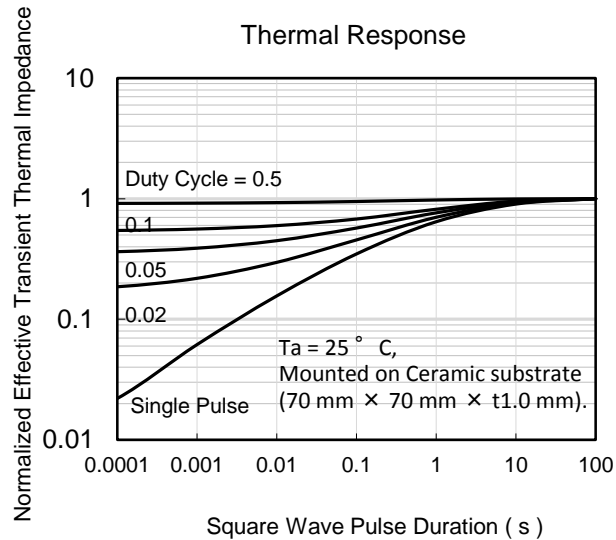
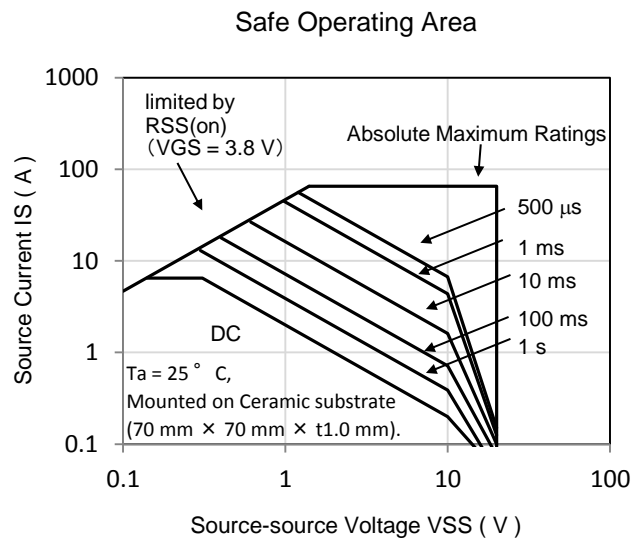
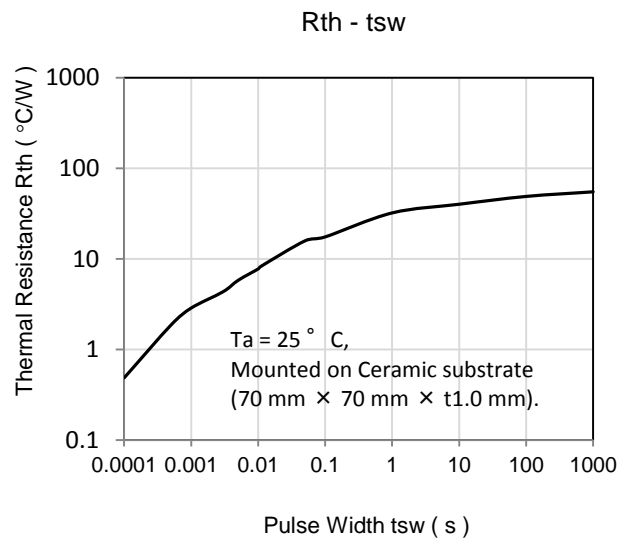
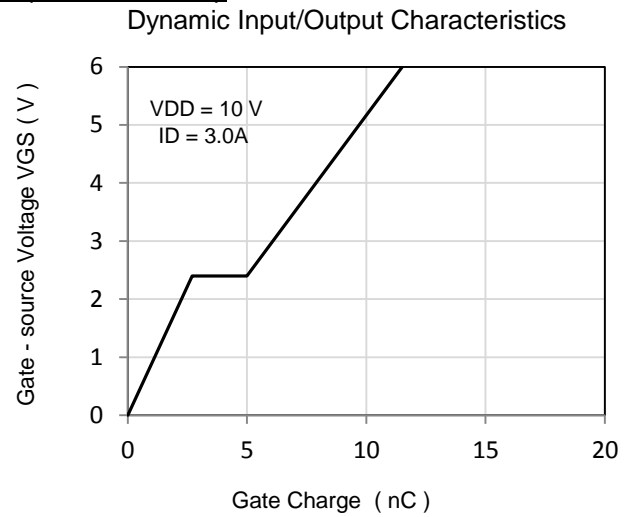
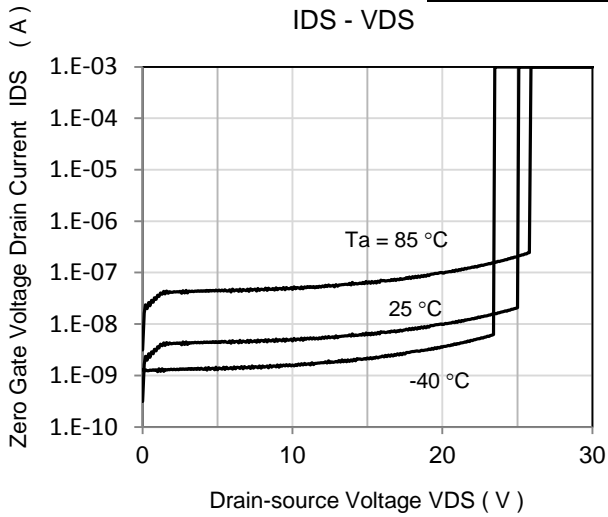


Technical Data (reference)



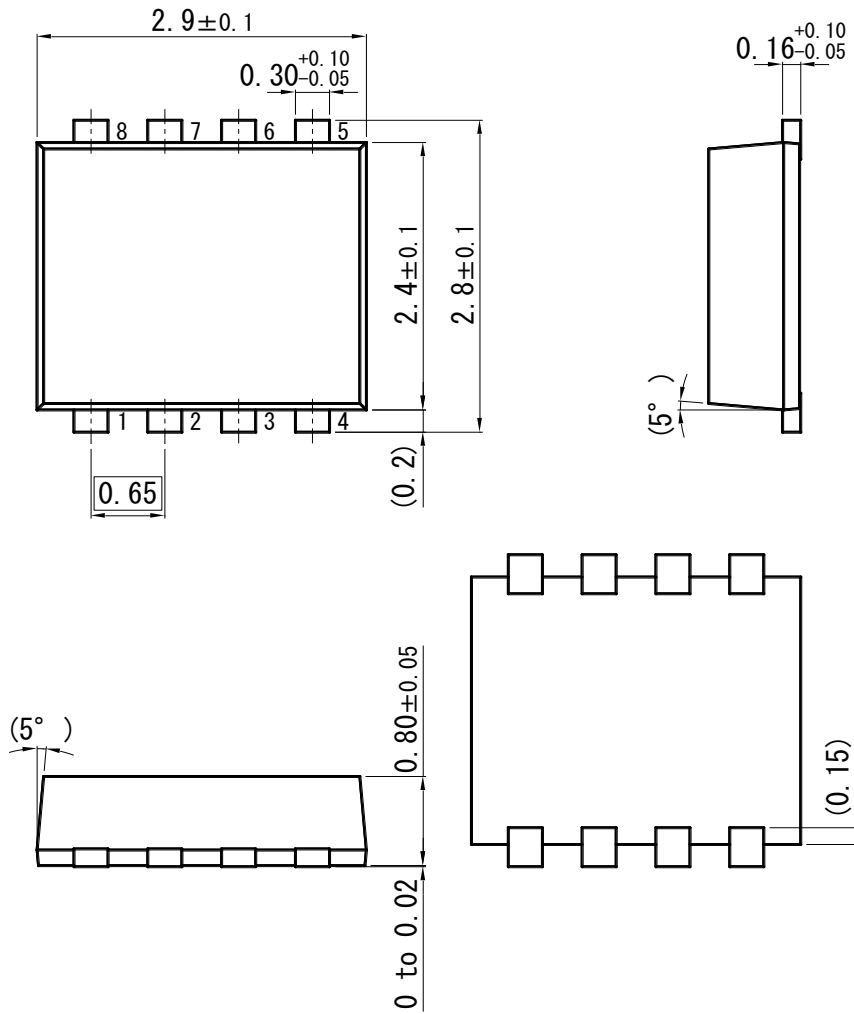


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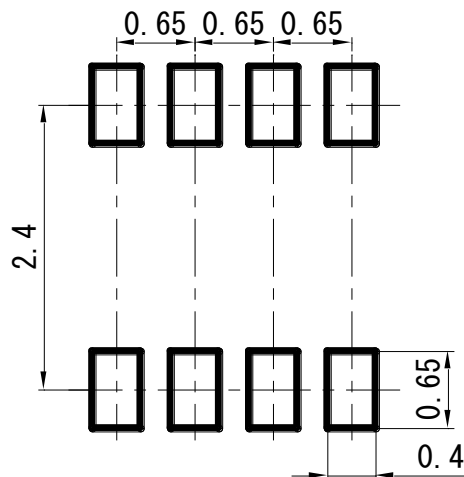


WMini8-F1

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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