Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

* Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan



FK9B0439ZL Single N-channel MOS FET

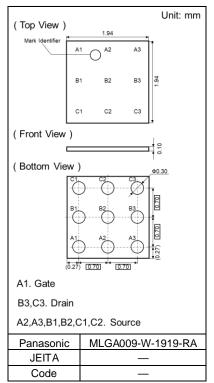
Features

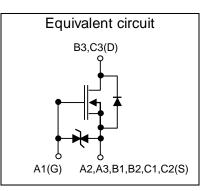
- Drain-source On-state Resistance : RDS(on) typ. = $9.5 \text{ m}\Omega$ (VGS = 10 V)
- CSP(Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL : Level 1)
- Automotive grade
- Marking Symbol : 5S

Packaging

Embossed type (Thermo-compression sealing) : 10,000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C					
Parameter	Symbol	Rating	Unit		
Drain-source Voltage		VDS	40	V	
Gate-source Voltage		VGS	+20 / -10	V	
Drain Current	DC	ID *1	7.1		
		ID *2	11.0	٨	
		ID *3	13.8	A	
	Pulsed *4	IDp	88.0		
Total Power Dissipation		PD ^{*1}	0.61		
		PD *2	1.60	W	
		PD *3	2.31		
Operating Junction and Storage Temperature Range		Tj,Tstg	-55 to +150	°C	





Thermal Characteristics Ta = 25 °C

Parameter	Symbol	Rating	Unit
	Rth1 *1	205	
Thermal Resistance (ch-a)	Rth2 *2	79	°C / W
	Rth3 *3	54	

 Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (79.2 mm² area, 35 μm thickness).
 *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).

FR4 board fully covered with copper pad $\,$ (616 mm^2 area, 35 μm thickness).

*3 Mounted on ceramic board (70 mm \times 70 mm \times t1.0 mm).

*4 t = 10 $\mu s,$ Duty Cycle \leq 1 %.

Panasonic

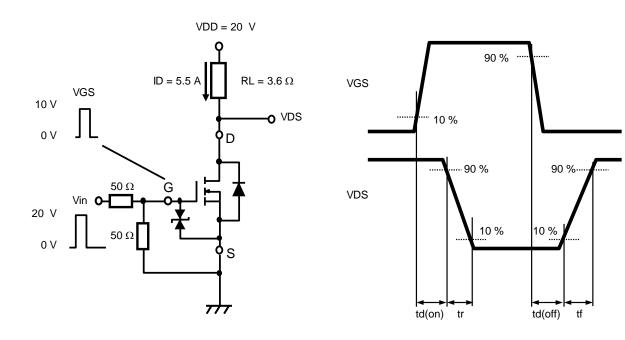
■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	40			V	
Zero Gate Voltage Drain Current	IDSS	VDS = 40 V, VGS = 0 V			10	μA	
Gate-source Leakage Current	IGSS	VGS = +16 V, VDS = 0 V			10	μA	
	1000	VGS = -8 V, VDS = 0 V			-10	μΑ	
Gate-source Threshold Voltage	Vth	ID = 1.85 mA, VDS = 10 V	1		3	V	
Drain-source On-state Resistance	RDS(on)1	ID = 2 A, VGS = 10 V	6	9.5	12	m O	
	RDS(on)2	ID = 2 A, VGS = 4.5 V	7	11	18	mΩ	
Body Diode Forward Voltage	VF(s-d)	IF = 2 A, VGS = 0 V		0.77	1.2	V	
Input Capacitance ^{*1}	Ciss			1500		pF	
Output Capacitance ^{*1}	Coss	VDS = 20 V, VGS = 0 V f = 1 MHz		190			
Reverse Transfer Capacitance ^{*1}	Crss			100			
Turn-on Delay Time *1,*2	td(on)	VDD = 20 V, VGS = 0 to 10 V		15		ns	
Rise Time ^{*1,*2}	tr	ID = 5.5 A		20			
Turn-off Delay Time *1,*2	td(off)	VDD = 20 V, VGS = 10 to 0 V		85			
Fall Time *1,*2	tf	ID = 5.5 A		55			
Total Gate Charge ^{*1}	Qg1	VDD = 20 V, VGS = 4.5 V ID = 11 A		14			
	Qg2			28		nC	
Gate-source Charge ^{*1}	Qgs	VDD = 20 V, VGS = 10 V ID = 11 A		4.5			
Gate-drain Charge ^{*1}	Qgd			5			

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

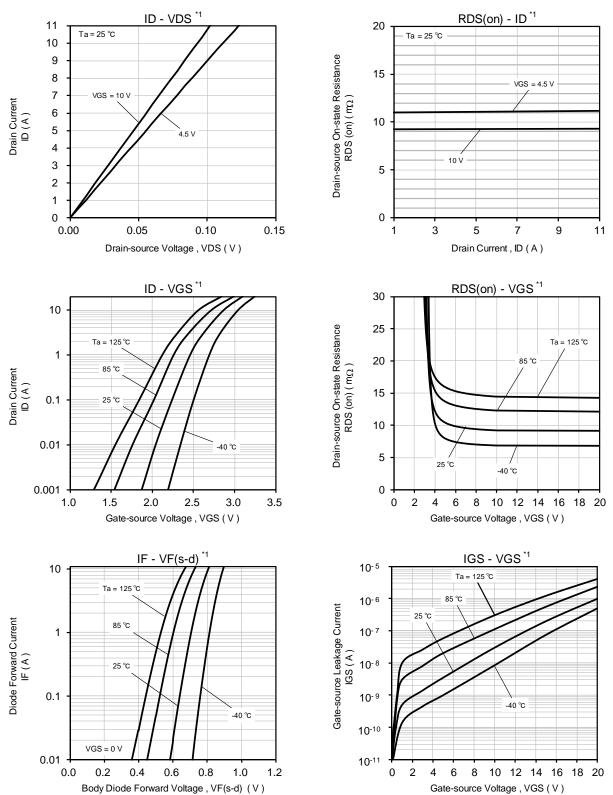
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



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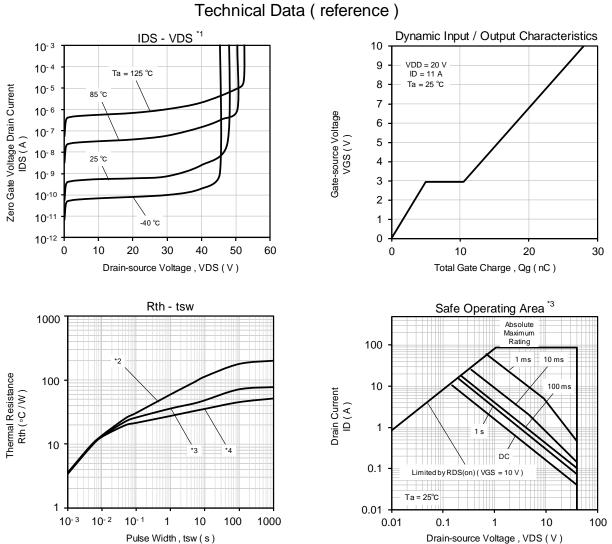
Technical Data (reference)



Established : 2017-09-07 Revised : 2020-11-11

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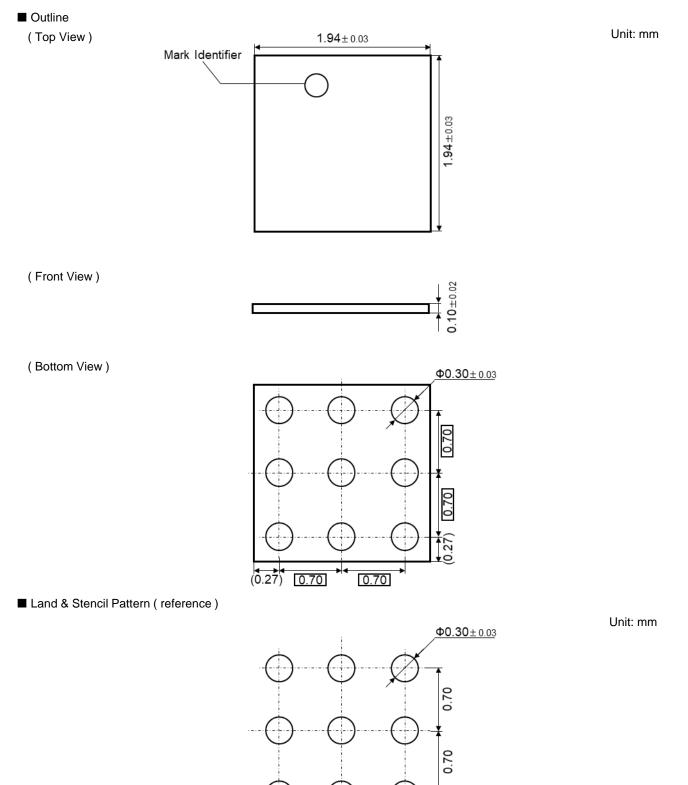


Note

- *1 Pulse measurement.
- $^{*}2$ Mounted on FR4 board (25.4 mm × 25.4 mm × 11.0 mm). FR4 board partially covered with copper pad (79.2 mm² area, 35 μm thickness).
- *3 Mounted on FR4 board (25.4 mm × 25.4 mm × 11.0 mm). FR4 board fully covered with copper pad (616 mm² area, 35 μ m thickness).
- *4 Mounted on ceramic board (70 mm \times 70 mm \times t1.0 mm).

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Datasheet Amendment History

Version	Status	Date	Change point(s)
1.0	Formal	2017.9.17	
2.0	Formal	2020.11.11	 Page2 Changed Measurement circuit for td(on), tr, td(off), and tf

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